



St. Francis Institute of Technology
DEPARTMENT OF ELECTRONICS AND TELECOMMUNICATION ENGINEERING

“Digital System Prototyping with FPGAs and Verilog/VHDL”
(5th Jan-9th Jan, 2026)

Report

A 30 Hrs. Value Added Course was conducted on “Digital System Prototyping with FPGAs and Verilog/VHDL” from 5th Jan-9th Jan, 2026. Following were resources person for the course.

- Dr. Ravindra Chaudhari, Course Co-Ordinator
- Ms. Snehal Lopes ,Course Co-Ordinator
- Ms. Madhavi Soni

As a part of Academic Activity of the EXTC Department, a series of sessions are arranged every semester to bridge the gap in the syllabus. Electronics and Telecommunication Engineering Department, had organized a 30 hrs. course on “Digital System Prototyping with FPGAs and Verilog/VHDL” during 5th Jan-9th Jan, 2026 for our third year (TE) EXTC students

Course objectives of ADD -ON Course:

1. To introduce the fundamentals of digital system design and FPGA-based prototyping
2. To familiarize students with FPGA architecture, design flow, and design tools
3. To develop proficiency in hardware description languages (Verilog/VHDL) for digital modeling
4. To enable the design and simulation of combinational and sequential digital circuits
5. To teach synthesis, implementation, and timing analysis for FPGA designs
6. To provide hands-on experience in programming and testing designs on FPGA boards
7. To encourage debugging, verification, and optimization of digital systems
8. To bridge the gap between theoretical digital concepts and real-time hardware implementation

Based on the **30-hour value-added course document** for the workshop titled “Digital System Prototyping with FPGAs and Verilog/VHDL” conducted by the Department of Electronics and Telecommunication Engineering, St. Francis Institute of Technology, the course is structured to progressively develop expertise in digital system design and FPGA-based prototyping. The program begins with an introduction to VLSI design flow and Verilog HDL fundamentals, and advances through FPGA architecture, design flow, and hands-on use of industry-standard tools such as Xilinx Vivado and ModelSim. Significant emphasis is placed on modelling, simulation, synthesis, and implementation of combinational and sequential circuits, including adders, flip-flops, counters, FSMs, memory elements, ALUs, and FIR filters. The course culminates in practical FPGA implementation and testing using the Basys-3 board, thereby bridging the gap between theoretical concepts and real-time hardware realization. The sessions are delivered by experienced resource persons **Dr. Ravindra Chaudhari, Ms. Snehal Lopes** and **Madhavi Soni** whose expertise ensures both strong conceptual understanding and effective hands-on learning for participants

21 Students registered for the course. The session was a big success, as all the participants had shown keen interest in this upcoming technology and asked many questions related to the topic. The Resource Person delivered an excellent session giving insights in Digital System Prototyping with FPGAs and Verilog/VHDL. This made students interested and motivated to take up projects in the said domain. The response and feedback from the participants, about the session was very good and as per the feedbacks, they would want to attend more sessions like this in future.

B. Images of the Session:





C. Student Attendance:

 ST. FRANCIS INSTITUTE OF TECHNOLOGY (Engineering College)		
DATE: 05/01/2026		PAGE NO.: 51
Course: Digital system Prototyping with FPGA's and verilog		
List of participants		
Name of the participant	Class	Signature
1) Ayush Maurya	TE EXTC A	Ayush
2) Abhishek Kharajia	TE EXTC A	Abhishek
3) Tammayee Desai	TE EXTC A	Tam
4) Unnati Mania	TE EXTC A	Unnati
5) Purnam Damaalkar	TE EXTC A	Purnam
6) Mukta Joshi	TE EXTC A	Mukta
7) Vyanna Doshi	TE EXTC A	Vyanna
8) Nisha Yande	TE EXTC B	Nisha
9) Lavanyaa Tharwal	TE EXTC B	Lavanyaa
10) Pravin Padaval	TE EXTC B	Pravin
11) Durvesh Bhakkar	TE EXTC A	Durvesh
12) Manas Wanjale	TE EXTC A	Manas
13) Nachiket Ghalsasi	TE EXTC A	Nachiket
14) Varun Wadke	TE EXTC A	Varun
15) Akash Singh	TE EXTC A	Akash
16) Ashaan Sheikh	TE EXTC B	Ashaan
17) Parth Tere-desai	TE EXTC B	Parth
18) Sateesh Chandra D. Gupta	TE EXTC A	Sateesh
19) Ninad B. Jadhav	TE EXTC A	Ninad
20) Harsh Kashyap	TE EXTC A	Harsh

5/01/25

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1)	Pravin. S. Padavai	243274	~~233~~	~~Padavai~~
2)	Varun S Wadke	243288		~~Vadake~~
3)	Ninad Tadhar	233024	T.E. EXTCA	~~Padhar~~
4)	Harsh Kashyap	233033	T.E. EXTCA-A	~~Harsh~~
5)	Manas Kinjale	233038	TE - A	~~Man~~
6)	Nikhilesh Gholsasi	233018	TE EXTCA	~~Nikhil~~
7)	Parth Tereadesai	233084	TE EXTCA	~~Parth~~
8)	Azhaan Shaikh	233072	TE EXTCA	~~Azha~~
9)	Lavanya Tharwal	233085	TE EXTCA	~~Lavanya~~
10)	Prithi Solanki	233081	TE EXTCA	~~Prithi~~
11)	Disha Yande	233088	TE EXTCA	~~Disha~~
12)	Purva Darnalkar	233007	TE EXTCA	~~Purva~~
13)	Mukta Joshi	233026	TE EXTCA	~~Mukta~~
14)	Vyoma Doshi	233012	TE EXTCA-A	~~Vyoma~~
15)	Urnati Mania	233041	TE-EXTCA	~~Urnati~~
16)	Tarmayee Desai	233009	TE-EXTCA	~~Tarmayee~~
17)	Sakshi Gaikwad	233016	TE-EXTCA	~~Sakshi~~
18)	Abhishek Kanjia	233030	TE-EXTCA	~~Abhishek~~
19)	Durvesh Bhalekar	233004	TE-EXTCA	~~Durvesh~~

30th's VAC on verilog

07/01/2026

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Date

1)	Kavanyaa Tharwal	233085	TE EXTC B	<u>Kavany</u>
2)	Disha Yande	233088	TE EXTC B	<u>D Yande</u>
3)	Prati Solanki	233081	TE EXTC B	<u>Prati</u>
4)	Pavith Tesiredesai	233084	TE EXTC B	<u>Pavith</u>
5)	Asiham Shailkh	233072	TE EXTC B	<u>Asiham</u>
6)	Purva Daundkar	233007	TE EXTC A	<u>Purva</u>
7)	Vyoma Doshi	233012	TE EXTC A	<u>Vyoma</u>
8)	Mukta Joshi	233026	TE EXTC A	<u>Mukta</u>
9)	Siddhesh Gupta	233021	TE EXTC A	<u>Siddhesh</u>
10)	Ninad B. Jedhar	233024	TE EXTC A	<u>Ninad</u>
11)	Harsh Kashyap	233033	TE EXTC-A	<u>Harsh</u>
12)	Nachiket Ghalassi	233018	TE EXTC A	<u>Nachiket</u>
13)	Manas Kinjale	233038	TE EXTC A	<u>Manas</u>
14)	Unnati Mania	233041	TE-EXTC-A	<u>Unnati</u>
15)	Sakshi Gaikwad	233016	TE-EXTC-A	<u>Sakshi</u>
16)	Pravin. S. Padaval	243274	TE-EXTC-B	<u>Pravin</u>
17)	Vrjun Wadke	243288	TE-EXTC-A	<u>Vrjun</u>
18)	Abhishek Kanaviya	233030	TE-EXTC A	<u>Abhishek</u>
19)	Tanmayee Desai	233009	TE EXTC A	<u>Tanmayee</u>
20)	Durvesh Bhalokar	233004	TE EXTC A	<u>Durvesh</u>

08th January 2026

classmate

Date

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Sign

Siddhesh

Class	Name	PID	
TE EXTCA	Siddhesh. D. Gupta	233021	
TE EXTCA	Ninad B. Jadhav	233024	<u>Ninad</u>
TE EXTCA	Harsh Kashyap	233033	<u>Harsh</u>
TE EXTCA	Vaman D. Wadke	243288	<u>Vaman</u>
TE EXTCB	Pravin. S. Padalkar	243274	<u>Pravin</u>
TE EXTCA	Nachiket Gholasi	233019	<u>Nachiket</u>
TE EXTC A	Manas Limjale	233038	<u>Manas</u>
TE EXTCA	Rukra Dandekar	233007	<u>Rukra</u>
TE EXTCA	Mukta Joshi	233026	<u>Mukta</u>
TE EXTCA	Vyoma Doshi		<u>Vyoma</u>
TE EXTCA	Abhishhek Kanjajiya	233030	<u>Abhishhek</u>
TE EXTCA	Tannayee Desai	233009	<u>Tannayee</u>
TE EXTC A	Durvesh Bhalokar	233004	<u>Durvesh</u>
TE EXTC A	Unnati Manja	233041	<u>Unnati</u>
TE EXTC B	Disha Yande	233088	<u>Disha</u>
TE EXTC B	Lavanyaa Jhanwal	233085	<u>Lavanyaa</u>
TE EXTC B	Prati Solanki	233081	<u>Prati</u>
TE EXTC B	Ashaan Shaikh	233073	<u>Ashaan</u>
TE EXTC B	Parth Teredesai	233084	<u>Parth</u>

09th January 2025

classmate

Date

Page

Ser No.	Name	PID	Class	Sign
01.	Siddhesh D. Gupta	233021	TE EXTCA	<u>Siddhesh</u>
2	Ninad B. Jadhav	233024	TE EXTCA	<u>Ninad</u>
3.	Harsh Mahesh Kashyap	233033	TE EXTCA	<u>Harsh</u>
4.	Manas Kinjale	233038	TE. EXTCA	<u>Manas</u>
5	Nachiket Ghalsasi	233018	TE EXTCA	<u>Nachiket</u>
6	Durvesh Bhalekar	233004	TE EXTCA	<u>Durvesh</u>
7	Abhishek Kanojiya	233030	TE EXTCA	<u>Abhishek</u>
8	Tanmayee Desai	233009	TE EXTCA	<u>Tanmayee</u>
9	Mukta Joshi	233026	TE EXTCA	<u>Mukta</u>
10.	Purva Damalkar	233007	TE EXTCA	<u>Purva</u>
11.	Vyoma Doshi	233012	TE - EXTCA	<u>Vyoma</u>
12.	Lavanya Tharwal	233085	TE EXTCA-B	<u>Lavanya</u>
13.	Prithi Solanki	233081	TE EXTCA-B	<u>Prithi</u>
14.	Disha Yande	233088	TE EXTCA-B	<u>Disha</u>
15.	Prithi Terdesai	233084	TE EXTCA-B	<u>Prithi</u>
16.	Aksham Shaitel	233073	TE EXTCA-B	<u>Aksham</u>
17.	Pravin. F. Padaval	243274	TE EXTCA-B	<u>Pravin</u>
18.	Varun D. Wadke	243288	TE EXTCA	<u>Varun</u>

D. Student Feedback:

	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P
	Timestamp	Resource Person	Name of the Student	Student PID	Class	Roll No	Branch	Email Id	Mobile Number	The session met my expectations	The content was helpful	The speaker had a good understanding of the topics	The speaker had good communication skills.	The session was worth of my	The length of the session	Suggestions Comments
1	1-5-2026 19:51:51	Ms.Snehal Lopes	Siddhesh Gupta	233021	TE EXTC A	30	Electronics and Telecommunication Engineering	Siddheshgupta7905@student.sfit.ac.in	7715875281	Good	Good	Good	Good	Good	Good	NA
2	1-5-2026 19:52:01	Ms.Snehal Lopes	Lavanyaa Tharwal	233085	TE EXTC B	59	Electronics and Telecommunication Engineering	lavanyaa12129@student.sfit.ac.in	8421403923	Very Good	Very Good	Very Good	Very Good	Very Good	Very Good	No
3	1-5-2026 19:52:24	Ms.Snehal Lopes	Manas kinjale	233038	TE EXTC A	54	Electronics and Telecommunication Engineering	Kinjalemanas1125@student.sfit.ac.in	9967343487	Good	Very Good	Very Good	Very Good	Very Good	Very Good	--
4	1-5-2026 20:05:13	Ms.Snehal Lopes	Parth Teredesai	233084	TE EXTC B	57	Electronics and Telecommunication Engineering	parth.teredesai@student.sfit.ac.in	9892549107	Good	Good	Good	Very Good	Good	Good	None
5	1-5-2026 20:10:39	Ms.Snehal Lopes	Purva Nilesh Daundkar	233007	TE EXTC A	12	Electronics and Telecommunication Engineering	daundkarpurva@student.sfit.ac.in	8879453379	Good	Very Good	Excellent	Very Good	Very Good	Good	-
6	1-5-2026 20:23:52	Ms.Snehal Lopes	Pravin padaval	243274	TE EXTC B	23	Electronics and Telecommunication Engineering	padavalpravin183@student.sfit.ac.in	9156899120	Very Good	Very Good	Very Good	Very Good	Very Good	Very Good	NA
7	1-5-2026 21:04:41	Ms.Snehal Lopes	Ninad Balkrishna Jadhav	233024	TE EXTC A	32	Electronics and Telecommunication Engineering	ninadj602@gmail.com	9969609686	Very Good	Excellent	Excellent	Excellent	Excellent	Excellent	The session was great. Just a small suggestion—if theory sessions can be explained along with practical sessions. Also, I would like to know how these concepts can be applied or be helpful in the upcoming mini projects.
8	1-5-2026 21:05:14	Ms.Snehal Lopes	Arhaan Shaikh	233073	TE EXTC B	45	Electronics and Telecommunication Engineering	arhaanshaikh020@student.sfit.ac.in	7718889234	Very Good	Very Good	Very Good	Very Good	Very Good	Very Good	-
9	1-5-2026 21:41:12	Ms.Snehal Lopes	Harsh Mahesh Kashyap	233033	TE EXTC A	47	Electronics and Telecommunication Engineering	harsh27077@student.sfit.ac.in	9326216756	Excellent	Excellent	Excellent	Excellent	Excellent	Excellent	NA
10	1-5-2026 21:52:53	Ms.Snehal Lopes	Varun Dinesh Wadke	243288	TE EXTC A	71	Electronics and Telecommunication Engineering	varunwadke@student.sfit.ac.in	8828509242	Excellent	Excellent	Excellent	Excellent	Excellent	Excellent	Nope

	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P
	Timestamp	Resource Person	Name of the Student	Student PID	Class	Roll No	Branch	Email Id	Mobile Number	The session met my expectations	The content was helpful	The speaker had a good understanding of the topics taught	The speaker had good communication skills.	The session was worth of my time.	The length of the session was appropriate	Suggestions Comments
1	1-8-2026 22:11:20	Dr.Ravindra Chaudhari	Manas kinjale	233038	TE EXTC A	54	Electronics and Telecommunication	Kinjalemanas1125@student.sfit.ac.in	9967343487	Very Good	Very Good	Very Good	Good	Very Good	Very Good	--
2	1-8-2026 22:12:39	Dr.Ravindra Chaudhari	Varun Dinesh Wadke	243288	TE EXTC A	71	Electronics and Telecommunication	varunwadke@student.sfit.ac.in	8828509242	Very Good	Very Good	Very Good	Very Good	Very Good	Very Good	Nope
3	1-8-2026 22:13:24	Dr.Ravindra Chaudhari	Durvesh Deshpale Bhalekar	233004	TE EXTC A	5	Electronics and Telecommunication	durveshbhalekar.sphu@student.sfit.ac.in	9152763021	Excellent	Excellent	Excellent	Excellent	Excellent	Excellent	Excellent
4	1-8-2026 22:16:24	Dr.Ravindra Chaudhari	Unnati Mania	233041	TE EXTC A	61	Electronics and Telecommunication	unnatimania777@student.sfit.ac.in	8828671806	Very Good	Very Good	Very Good	Very Good	Very Good	Very Good	-
5	1-8-2026 22:16:30	Ms.Snehal Lopes	Parth Teredesai	233084	TE EXTC B	57	Electronics and Telecommunication	parth.teredesai@student.sfit.ac.in	9892549107	Good	Good	Good	Good	Good	Good	-
6	1-8-2026 22:22:30	Dr.Ravindra Chaudhari	Siddhesh Gupta	233021	TE EXTC A	30	Electronics and Telecommunication	siddheshgupta7905@gmail.com	7715875281	Good	Good	Good	Good	Good	Good	NOT APPLICABLE
7	1-8-2026 22:25:07	Dr.Ravindra Chaudhari	Nachiket Ghalsai	233018	TE EXTC A	25	Electronics and Telecommunication	ghalsai.nachiket@student.sfit.ac.in	8976194901	Good	Good	Good	Good	Good	Good	-
8	1-8-2026 22:27:31	Dr.Ravindra Chaudhari	Tanmayes Desai	233009	TE EXTC A	14	Electronics and Telecommunication	tdesai2005@student.sfit.ac.in	9892021547	Very Good	Excellent	Very Good	Excellent	Excellent	Very Good	-
9	1-8-2026 22:37:43	Dr.Ravindra Chaudhari	Lavanyaa Tharwal	233085	TE EXTC B	59	Electronics and Telecommunication	lavanyaa12129@student.sfit.ac.in	8421403923	Very Good	Good	Good	Very Good	Very Good	Very Good	No
10	1-8-2026 22:38:52	Dr.Ravindra Chaudhari	Arhaan Shaikh	233073	TE EXTC B	45	Electronics and Telecommunication	arhaanshaikh020@student.sfit.ac.in	7718889234	Very Good	Very Good	Very Good	Very Good	Very Good	Very Good	-
11	1-8-2026 22:57:40	Dr.Ravindra Chaudhari	Pravin padaval	243274	TE EXTC B	23	Electronics and Telecommunication	padavalpravin183@student.sfit.ac.in	9156899120	Very Good	Very Good	Very Good	Excellent	Very Good	Very Good	NA
12	1-8-2026 23:15:59	Dr.Ravindra Chaudhari	Vyoma Doshi	233012	TE EXTC A	17	Electronics and Telecommunication	vyomadoshi11@student.sfit.ac.in	7777098422	Very Good	Very Good	Very Good	Very Good	Very Good	Very Good	No suggestions
13	1-8-2026 23:34:34	Dr.Ravindra Chaudhari	Harsh Mahesh Kashyap	233033	TE EXTC A	47	Electronics and Telecommunication	harsh27077@student.sfit.ac.in	9326216756	Good	Good	Good	Good	Very Good	Good	NA
14	1-9-2026 0:45:52	Dr.Ravindra Chaudhari	Ninad Balkrishna Jadhav	233024	TE EXTC A	32	Electronics and Telecommunication Engineering	ninadj602@gmail.com	9969609686	Excellent	Very Good	Excellent	Excellent	Excellent	Very Good	Great session, but a little exhausting
15	1-9-2026 9:04:28	Dr.Ravindra Chaudhari	Purva Nilesh Daundkar	233007	TE EXTC A	12	Electronics and Telecommunication	daundkarpurva@student.sfit.ac.in	8879453379	Very Good	Very Good	Excellent	Excellent	Very Good	Good	-

E. Result Analysis:

A) Quiz Question paper(s):

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Final Test

Final Test

30 Hour VAC on Digital System Prototyping with FPGAs and Verilog/VHDL *

* Indicates required question

1. Email *

2. Name: *

3. 1. What is the fundamental building block of an FPGA that implements logic functions? * 2 points

Mark only one oval.

- ☐ A) Microprocessor
- ☐ B) Configurable Logic Block (CLB) / Logic Element (LE)
- ☐ C) Logic Gate Array
- ☐ D) Transistor Switch

4. 2. Which component in an FPGA is responsible for providing fixed-function mathematical acceleration? * 2 points

Mark only one oval.

- ☐ A) Flip-flops
- ☐ B) I/O Blocks
- ☐ C) DSP Slices
- ☐ D) Routing Matrix

<https://docs.google.com/forms/d/10MTDc8E2U7pgZ2BwVWHNLhPwMapao1ZOG7M0nRo/edit>

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Final Test

5. 3) In the FPGA design flow, what is the purpose of "Synthesis"? *

2 points

Mark only one oval.

- ☐ A) Converting HDL code into a netlist of logic gates.
- ☐ B) Assigning physical pins to signals.
- ☐ C) Generating the final bitstream file.
- ☐ D) Testing the code for syntax errors only.

6. 4) Which stage of the FPGA design flow determines the physical placement of logic cells and the routing of wires between them? * 2 points

Mark only one oval.

- ☐ A) RTL Simulation
- ☐ B) Synthesis
- ☐ C) Implementation (Place and Route)
- ☐ D) Bitstream Generation

7. 5) In Verilog, which keyword is used to describe a block of code that executes concurrently and is triggered by signal changes? * 2 points

Mark only one oval.

- ☐ A) initial
- ☐ B) always
- ☐ C) function
- ☐ D) task

<https://docs.google.com/forms/d/10MTDc8E2U7pgZ2BwVWHNLhPwMapao1ZOG7M0nRo/edit>

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8. 6) What is the effect of using a "non-blocking assignment" (<=) in Verilog? * 2 points

Mark only one oval.

- ☐ A) The assignment happens immediately.
- ☐ B) It is used primarily for combinational logic.
- ☐ C) All assignments occur simultaneously at the end of the time step.
- ☐ D) It prevents the use of clocks.

9. 7) What is a "Testbench" in the context of HDL? * 2 points

Mark only one oval.

- ☐ A) A physical piece of hardware used for debugging.
- ☐ B) A non-synthesizable HDL module used to provide stimulus to the Design Under Test (DUT).
- ☐ C) The software used to download code to the FPGA.
- ☐ D) A specialized logic analyzer.

10. 8) What is a "Constraint File" (e.g., .XDC or .UCF) used for? * 2 points

Mark only one oval.

- ☐ A) Limiting the number of lines in the HDL code.
- ☐ B) Mapping HDL signals to specific physical pins and defining clock speeds.
- ☐ C) Compressing the bitstream.
- ☐ D) Storing simulation results.

11. 9) What is the main advantage of an FPGA over an ASIC for prototyping? * 2 points

Mark only one oval.

- ☐ A) Higher performance.
- ☐ B) Lower unit cost for mass production.
- ☐ C) Reconfigurability and shorter time-to-market.
- ☐ D) Lower power consumption.

12. 10) "Look-Up Tables" (LUTs) in FPGAs are primarily used to implement: * 2 points

Mark only one oval.

- ☐ A) Large memory arrays.
- ☐ B) Combinational logic functions.
- ☐ C) Clock signals.
- ☐ D) Physical I/O pins.

13. 11) What is "JTAG" commonly used for in FPGA prototyping? * 2 points

Mark only one oval.

- ☐ A) High-speed data streaming.
- ☐ B) Programming the FPGA and on-chip debugging.
- ☐ C) Connecting the FPGA to a monitor.
- ☐ D) Powering the FPGA board.

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Final Test

14. 12) What does the acronym "EDA" stand for in the context of electronics? * 2 points

Mark only one oval.

- ☐ A) Electronic Device Architecture
☐ B) Electronic Design Automation
☐ C) Embedded Digital Application
☐ D) Electrical Design Analysis

15. 13) Which of the following is considered a "Back-End" EDA task? * 2 points

Mark only one oval.

- ☐ A) RTL Coding
☐ B) Behavioral Simulation
☐ C) Floorplanning and Placement
☐ D) Logic Synthesis

16. 14) Vivado is the successor to which previous Xilinx design tool? * 2 points

Mark only one oval.

- ☐ A) ModelSim
☐ B) Xilinx ISE
☐ C) Synplify Pro
☐ D) Quartus Prime

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Final Test

17. 15) Which Vivado feature allows users to convert C, C++, or SystemC code directly into RTL? * 2 points

Mark only one oval.

- ☐ A) Vivado Simulator
☐ B) IP Integrator
☐ C) Vivado HLS (High-Level Synthesis)
☐ D) Logic Analyzer

18. 16) In the Vivado "Flow Navigator," which step follows Synthesis? * 2 points

Mark only one oval.

- ☐ A) Project Manager
☐ B) Implementation
☐ C) Bitstream Generation
☐ D) Simulation

19. 17) Which file extension is generated by Vivado to program a Xilinx FPGA? * 2 points

Mark only one oval.

- ☐ A) .sof
☐ B) .bit
☐ C) .hex
☐ D) .bin

20. 18) ModelSim is primarily used for which stage of the design flow? *

2 points

Mark only one oval.

- ☐ A) Place and Route
☐ B) Physical Synthesis
☐ C) Functional and Timing Simulation
☐ D) Board Layout

21. 19) Which ModelSim window displays the change of signal values over time? *

2 points

Mark only one oval.

- ☐ A) Transcript Window
☐ B) Structure Window
☐ C) Wave Window
☐ D) Objects Window

22. 20) What is the difference between "Functional Simulation" and "Timing Simulation"? *

2 points

Mark only one oval.

- ☐ A) Functional checks logic only; Timing includes gate and wire delays.
☐ B) Functional is done after Synthesis; Timing is done before.
☐ C) Functional is only for VHDL; Timing is only for Verilog.
☐ D) There is no difference.

23. 21) What does a "Force" command do in a simulator? *

2 points

Mark only one oval.

- ☐ A) It deletes a signal from the waveform.
☐ B) It manually overrides a signal to a specific value regardless of the logic.
☐ C) It speeds up the simulation clock.
☐ D) It forces the tool to bypass synthesis errors.

24. 22) Which standard format is used to exchange timing information between EDA tools for Timing Simulation? *

2 points

Mark only one oval.

- ☐ A) VCD (Value Change Dump)
☐ B) SDF (Standard Delay Format)
☐ C) XML
☐ D) JSON

25. 23) In ModelSim, the work library is: *

2 points

Mark only one oval.

- ☐ A) The default library where compiled design units are stored.
☐ B) A library containing standard IEEE components only.
☐ C) The folder where the software is installed.
☐ D) A library for non-synthesizable code only.

26. 24) Which of the following is the correct way to declare an 8-bit wire in Verilog? * 2 points

Mark only one oval.

- ☐ A) wire [8:0] bus;
☐ B) wire [7:0] bus;
☐ C) wire bus[8];
☐ D) bit [7:0] wire;

27. 25) What is the default initial value of a reg data type in simulation? * 2 points

Mark only one oval.

- ☐ A) 0
☐ B) 1
☐ C) X (Unknown)
☐ D) Z (High Impedance)

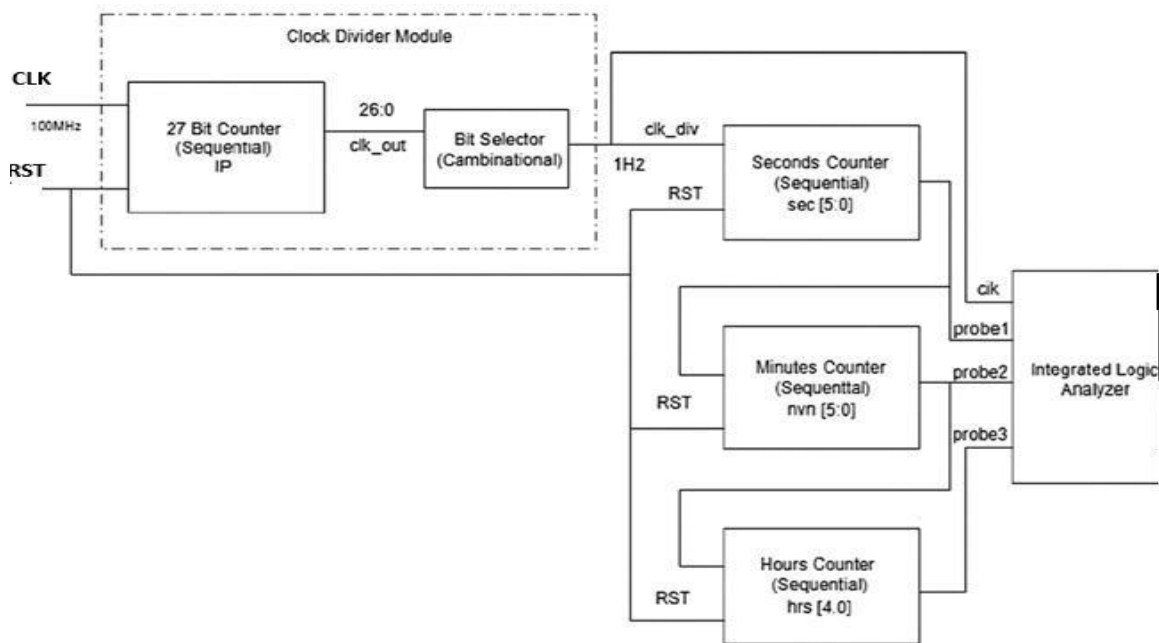
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Assignments/Projects assigned:

This project implements a digital clock system that counts seconds, minutes, and hours using sequential logic components. The system is driven by a high-frequency 100 MHz clock, which is first divided down to a 1 Hz signal using a **Clock Divider** module. This divided clock signal is then used to drive the entire timekeeping system.

The **Seconds Counter** counts from 0 to 59 and triggers the **Minutes Counter**, which also counts from 0 to 59. The **Hours Counter** increments every 60 minutes and can count up to 23.



Objectives:

1. All the blocks provided in the block diagram are supposed to be separate module files.
2. The clock divider module should have a 27 bit counter and a bit selector in which you can use the assign statement. This module is responsible for driving the clock of the whole circuit.
3. You should note that the clock which is responsible for driving the ILA should be the clock that has been divided and not the 100MHz clock.
4. A single ILA with 3 probes should be used to check the clock timings accordingly.

Assessment Result:

Digital System Prototyping with FPGAs and Verilog/VHDL (Responses)						
File Edit View Insert Format Data Tools Extensions Help						
100% 123 Roboto 10						
B8 daundkarpurva@student.sfit.ac.in						
	A	B	C	D	E	F
	Form_Responses					
1	Timestamp	Email Address	#	Score	Name:	1. What is the fundamental building block of i v 2. Which comp v 3) In the FPGA design
2	1/9/2026 15:04:54	vedantkachare5@student.sfit.ac.in	46	Vedant Kachare	B) Configurable Logic Block (CLB) / Logic Elemen	C) DSP Slices
3	1/9/2026 15:12:40	roshantalaviya905@student.sfit.ac.in	46	Roshan Talaviya	B) Configurable Logic Block (CLB) / Logic Elemen	C) DSP Slices
4	1/9/2026 15:44:31	abhishek2807.k@student.sfit.ac.in	44	Abhishek kanojiya	B) Configurable Logic Block (CLB) / Logic Elemen	C) DSP Slices
5	1/9/2026 15:45:25	unnatimania777@student.sfit.ac.in	50	Unnati Mania	B) Configurable Logic Block (CLB) / Logic Elemen	A) Flip-flops
6	1/9/2026 15:47:54	disha.yande2006@student.sfit.ac.in	42	Disha Yande	C) Logic Gate Array	C) DSP Slices
7	1/9/2026 15:49:35	varunwadke@student.sfit.ac.in	46	Varun Dinesh Wadke	B) Configurable Logic Block (CLB) / Logic Elemen	C) DSP Slices
8	1/9/2026 15:51:20	daundkarpurva@student.sfit.ac.in	48	Purva Nilesh Daundkar	B) Configurable Logic Block (CLB) / Logic Elemen	A) Flip-flops
9	1/9/2026 15:51:23	vyomadoshi11@student.sfit.ac.in	48	Vyoma Doshi	B) Configurable Logic Block (CLB) / Logic Elemen	A) Flip-flops
10	1/9/2026 15:54:48	mauryaayush602@student.sfit.ac.in	44	Ayush Maurya	B) Configurable Logic Block (CLB) / Logic Elemen	C) DSP Slices
11	1/9/2026 15:56:46	sakshigaikwad933@gmail.com	50	Sakshi Gaikwad	B) Configurable Logic Block (CLB) / Logic Elemen	A) Flip-flops
12	1/9/2026 16:02:04	padavalpravin183@student.sfit.ac.in	46	pravin padaval	B) Configurable Logic Block (CLB) / Logic Elemen	C) DSP Slices
13	1/9/2026 16:58:16	siddheshgupta7905@gmail.com	46	Siddhesh Gupta	B) Configurable Logic Block (CLB) / Logic Elemen	C) DSP Slices
14	1/9/2026 18:32:38	harsh27077@student.sfit.ac.in	46	Harsh Mahesh Kashyap	B) Configurable Logic Block (CLB) / Logic Elemen	C) DSP Slices
15	1/9/2026 19:21:00	lavanyaa12129@student.sfit.ac.in	46	Lavanyaa Tharwal	B) Configurable Logic Block (CLB) / Logic Elemen	C) DSP Slices
16	1/9/2026 19:24:27	vinaykumar1255@student.sfit.ac.in	46	Vinay Kumar	B) Configurable Logic Block (CLB) / Logic Elemen	C) DSP Slices

Marks	No. of Students
above 90%	21
between 81% to 90%	-
between 75% to 80%	-
Below 75%	-

Comment on the Result Analysis stating the impact of the course: It was observed that after attending the seminar, a significant improvement was seen in students' performance, as many were able to answer a greater number of questions. Students developed a clear understanding of FPGA architecture and the role of Verilog HDL in digital system design. They were able to write synthesizable Verilog code for basic and intermediate digital circuits, simulate and verify designs using FPGA development tools such as Vivado, and successfully implement Verilog designs on FPGA boards to observe real-time hardware outputs. Additionally, students were capable of designing and testing mini projects such as counters, multiplexers, finite state machines (FSMs), and arithmetic circuits.

Sample Certificate copy



Dr. Ravindra Chaudhari and Ms. Snehal Lopes
 (Course Coordinator)

Dr. Kevin Noronha
 (Convener and HOD-EXTC)